

Fastwel
AIC324

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AIC324

Analog and Discrete Input/Output Module

User Manual

Preliminary

Original document: IMES 469535.110 v.1.2

1 Specifications

Main Features

System controller interface – PC/104 (ISA 16 bit)

Pass-through PCI bus

32 analog inputs; ADC 16 bit; 250 kHz; $\pm 10\text{ V} \dots \pm 0.625\text{ V}$

4 analog outputs; DAC 16 bit; 6 s; $\pm 10\text{ V} \dots \pm 2.5\text{V}$;
programmable calibration of analog circuits

24 discrete input/output channels; 3.3 V or 5 V CMOS;
support for 16-bit and 32-bit counters; electrostatic protection of outputs

Analog/discrete isolation: 500 V

Supported operating systems: Fastwel DOS, Linux, QNX

Analog input

- 32 single-wire or 16 differential voltage or current input channels with group galvanic isolation;
- Single-wire, differential or mixed connection of input signals;
- 16-bit digital-analog converter;
- AD converter conversion time 4 μs /channel;
- Input voltage range $\pm 10\text{ V}$, 0–10 V;
- Input current range: 0–20 mA;
- Programmable input signal gains: 1, 2, 4, 8, 16;
- Input resistance: $>1\text{ M}\Omega$ (voltage); 249 Ω (current);
- Programmable autocalibration of input signal measurement ranges;
- Programmable auto scanning of inputs;
- FIFO buffer for 2048 words;
- Individual overvoltage protection of channels $\pm 40\text{ V}$ (DC).

Analog output

- 4 single-wire voltage output channels with group galvanic isolation;
- 16-bit digital-analog converter;
- DAC establishment time 6 μs ;
- Programmable selection of output signals conversion range:
 $\pm 10\text{ V}$, $\pm 5\text{ V}$, $\pm 2.5\text{ V}$, 0–10 V, 0–5 V;
- Programmable autocalibration of output signal conversion ranges;
- FIFO buffer for 2048 words;
- Operation in signal generator mode;
- Individual protection of channels from static electricity (ESD).

Discrete input/output

- 24 + 6 + 7 TTL/CMOS level compatible input/output channels;
- 7 galvanically isolated channels; Discrete inputs/outputs configuration compatibility with 8255 (Mode 0 and mode 1 channel A);
- Group pull-down or pull-up of discrete outputs;
- 8254 type timer available.

Additional features

- Automatic installation of calibrated ADC and DAC ranges when powered on;
- Built-in current measurement transistors with "floating" ground;
- 16/32 bit timer (8254 type), ADC start enabled;
- External ADC bit synchronization capability;
- Synchronous operation of ADCs on several boards capability;
- 16-digit timer for forming signals analogous to 8254;
- 10 shared hardware interrupt lines;
- 2 shared DMA channel request lines.

System bus

- 8/16-bit ISA bus;
- PC104+ feedthrough connector.

Module power supply

- Direct current power supply voltage: +5V \pm 5%;
- Consumed power (without external devices): 450 mA;
- Insulation voltage: 1000 V.

Operating conditions

- Operating temperatures range: -40°C to $+85^{\circ}\text{C}$;
- Relative humidity: maximum 95% at $+25^{\circ}\text{C}$;

Storage temperature

- -55°C to $+85^{\circ}\text{C}$.

MTBF

- At least 100000 hrs.

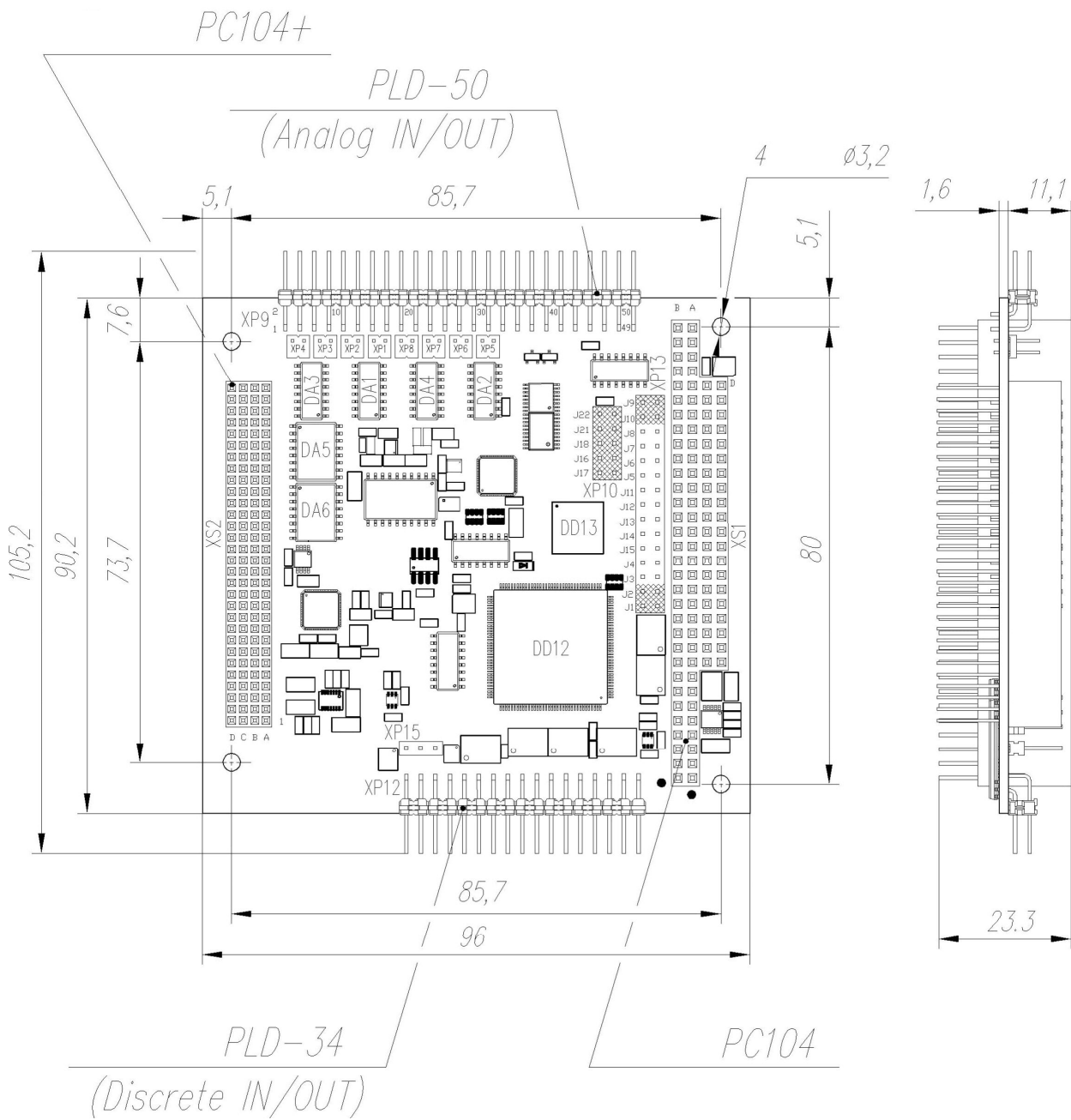
Protective coating

Dimensions

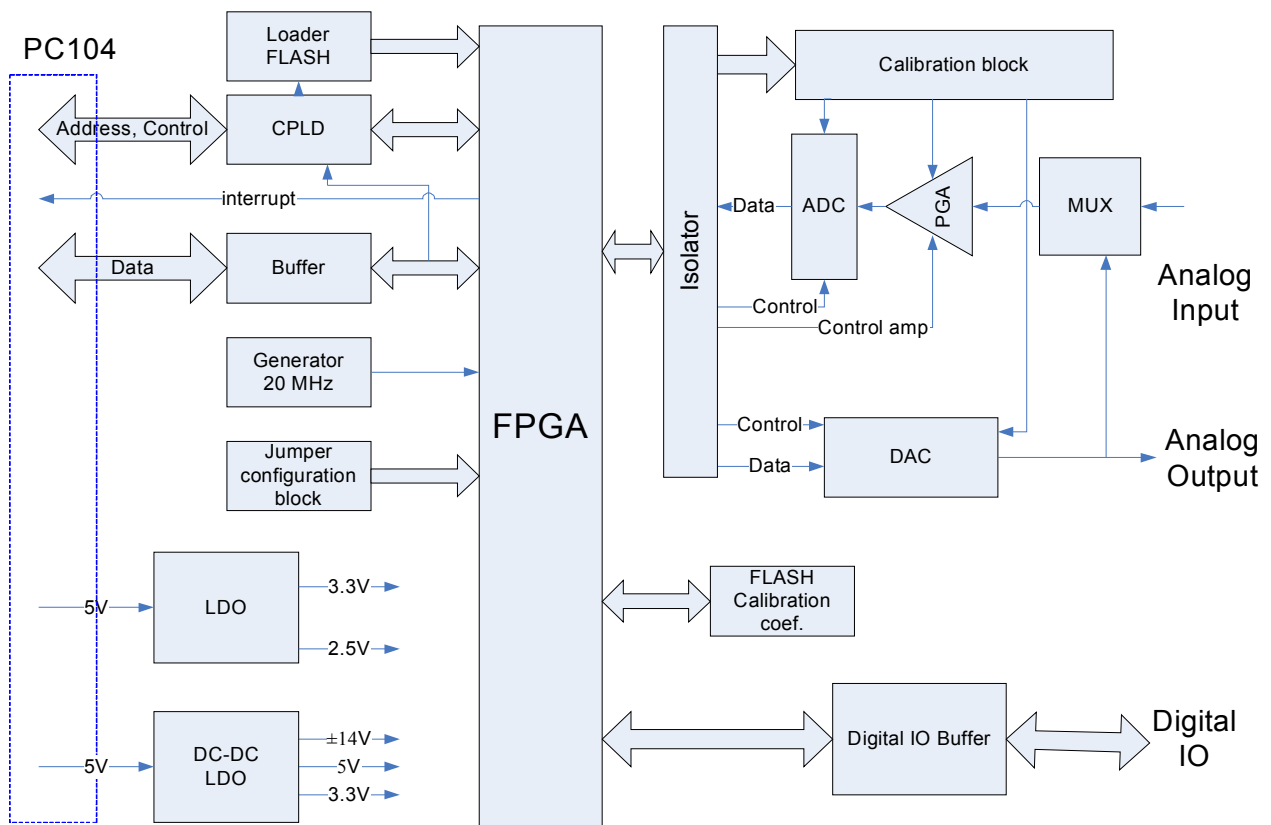
- 93×96×23 mm.

2 Description

2.1 Main Components Layout



2.2 Block Diagram



2.3 Peripheral Devices Connection

Table 1
Connectors

Name on PCB	Function	# of Contacts
XS1 (PC104)	Connection of PC104 expansion module via ISA bus	104
XS2 (PC104+)	Pass-through connector; installed for PC104+ system assembly convenience. Not connected to the circuitry of the module.	120
XP12 (Discrete IN/OUT)	30 discrete I/O lines	34
XP9 (Analog IN/OUT)	32 analog input lines, 4 analog output lines, 4 discrete input lines, 3 discrete output lines	50
XP13	Interrupt and DMA channel number setting	30
XP10	Configuring of ADC input channels types and base address	10
XP15	Setting the discrete inputs/outputs group pull-up	3
XP1 - XP8	Connection of current measurement resistors to differential ADC channels	4

Table 2
LED Indication

Name on PCB	Function	Color
VD1 (LED1)	User LED	Yellow

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3 Connectors and Ports

3.1 Analog Connector

Table 3
XP9 Analog Connector Pinout

AGND	1	2	AGND
Vin0 / 0+	3	4	Vin16 / 0-
Vin1 / 1+	5	6	Vin17 / 1-
Vin2 / 2+	7	8	Vin18 / 2-
Vin3 / 3+	9	10	Vin19 / 3-
Vin4 / 4+	11	12	Vin20 / 4-
Vin5 / 5+	13	14	Vin21 / 5-
Vin6 / 6+	15	16	Vin22 / 6-
Vin7 / 7+	17	18	Vin23 / 7-
Vin8 / 8+	19	20	Vin24 / 8-
Vin9 / 9+	21	22	Vin25 / 9-
Vin10 / 10+	23	24	Vin26 / 10-
Vin11 / 11+	25	26	Vin27 / 11-
Vin12 / 12+	27	28	Vin28 / 12-
Vin13 / 13+	29	30	Vin29 / 13-
Vin14 / 14+	31	32	Vin30 / 14-
Vin15 / 15+	33	34	Vin31 / 15-
Vout DAC3	35	36	Vout DAC2
Vout DAC1	37	38	Vout DAC0
Vref out	39	40	AGND
A/D Conversion	41	42	Ctr2 out/ Dout 2
Dout 1	43	44	Ctr0 out/ Dout 0
Extclk/Din 3	45	46	ExtGate / Din 2
Gate 0/ Din 1	47	48	Clk0 / Din0
+5V	49	50	DGND

Table 4
Designation of XP9 Signals

Name	Function
Vin 0/0+ ~ Vin 15/15+	Analog inputs: 0-15 single-wire inputs/0-15 positive diff.
Vin 16/0- ~ Vin 31/15-	Analog inputs: 16-31 single-wire inputs/0-15 neg. diff.
Vref out	Reference +5V output. Do not use as power voltage.
Vout DAC 0-3	Analog outputs
A/D Conversion	Pulse to start A/D conversion (output)

Name	Function
Dout 2- 0	Galvanically isolated discrete outputs combined with a pulse counter
Din 3 – 0	Galvanically isolated discrete inputs combined with a pulse counter or ADC startup
ExtClk	External ADC startup
ExtGate	Input gate latches Ctr 1&2 of 8254 timers module
Gate 0	Input gate latch Ctr0 of 8254 timers module
Clk 0	External clock input for timer 0 (8254 module) operation
+5V	Output of galvanically isolated +5V
ADND	Analog ground of galvanically isolated analog highway
DGND	Discrete ground of galvanically isolated analog highway

3.2 Discrete Connector

Table 5
Pinout of Discrete Connector (XP12)

A7	1	2	A6
A5	3	4	A4
A3	5	6	A2
A1	7	8	A0
B7	9	10	B6
B5	11	12	B4
B3	13	14	B2
B1	15	16	B0
C7	17	18	C6
C5	19	20	C4
C3	21	22	C2
C1	23	24	C0
Latch	25	26	Ack
D0	27	28	D1
D2	29	30	D3
D4	31	32	D5
+5V	33	34	DGND

Table 6
Designation of XP12 Signals

Name	Function
A7 – A0	Discrete I/O port A
B7 – B0	Discrete I/O port B
C7 – C0	Discrete I/O port C
D5 – D0	Discrete additional I/O port D
Latch	Latch input, active level high (port A, mode 1)
Ack	Acknowledgement output, active level high (port A, mode 1)
+5V	+5V discrete power
DGND	Discrete ground of PC104 bus

3.3 Registers Mapping

+0	W	ADC conversion software start						
If ADC is not in Busy state (AD_BUSY high), writing of any value to the register leads to starting of ADC conversion.								

+0	R	Reading of the lower data byte from ADC						
Bit #	7	6	5	4	3	2	1	0
Name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
AD7 – 0 – ADC data from 7 to 0 bits.								

+1	R	Reading of the higher data byte from ADC						
Bit #	7	6	5	4	3	2	1	0
Name	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
AD15 – 8 - ADC data from 15 to 8 bits. *When using 8-bit module access commands, higher byte should be read first, then lower byte.								

+2	RW	Lower ADC channel number in scan mode.						
Bit #	7	6	5	4	3	2	1	0
Name	x	x	x	CL4	CL3	CL2	CL1	CL0
Lower ADC channel number in scan mode. Writing to this register leads to setting of the channel at the module. Channel number can be from 0 to 31.								

+3	RW	Higher ADC channel number in scan mode.						
Bit #	7	6	5	4	3	2	1	0
Name	x	x	x	CH4	CH3	CH2	CH1	CH0
Higher ADC channel number in scan mode. Channel number can be from 0 to 31.								

+4	W	ADC control						
Bit #	7	6	5	4	3	2	1	0
Name	FIFOEN	ADINTE	SCANEN	x	x	x	x	FIFORST
SCANEN (bit 5) – Enable ADC channels scan mode. ADINTE (bit 6) – Enable interrupt from ADC. FIFOEN (bit 7) – Enable FIFO mode when using ADC. If interrupt is enabled, it will occur when TF flag is set to 1. If this mode is disabled and interrupt from ADC is enabled, it will occur each time on ADC conversion. Bit FIFORST – Reset FIFO pointers.								

+4	R	ADC status						
Bit #	7	6	5	4	3	2	1	0
Name	FIFOEN	WAIT	STS	0	EF	TF	FF	OVR

EF, TF, FF, OVF – ADC FIFO status bits: Empty FIFO, FIFO threshold reached, FIFO overflow.
 STS (bit 5) – ADC status: if = 1 the conversion in process or channels scan mode in process.
 WAIT (bit 6) = 0 – ADC conversion enabled; = 1 – conversion start is not allowed, the time is needed for setting a signal when a channel is changed, gain or range is switched. The waiting time is about 10 microseconds.

+5	R	DAC status						
Bit #	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	DACBUSY

DACBUSY bit indicates that data is being transferred to DAC. At this moment write to the registers 5 and 6 is disabled.

+5	W	DAC control						
Bit #	7	6	5	4	3	2	1	0
Name	WGSTRT	WGPS	WGRST	WGINC	DASIM	DAGEN	DACH1	DACH0

Bits DACH1-0 set current DAC channel in operation (0 to 3).
 Bit DAGEN – if = 1, write the set data in FIFO along with the channel number.
 Bit DASIM – if = 0, when writing Register 5, the data is transferred to DAC and set at DAC output; if = 1, write to buffer occurs without output to DAC.
 Bit WGINC – Write the data and increment the address counter in buffer. Manual mode.
 Bit WGRST – Reset the generator buffer address.
 Bit WGPS – Pause the generator. During pause, bit WGRST can be used to reset the generator.
 Bit WGSTRT – Generator start in any mode.

+6	R	Update DAC data for all 4 channels						
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Update DAC data for all 4 channels.

+6	W	Write 8 lower DAC bits						
Bit #	7	6	5	4	3	2	1	0
Name	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

8 lower DAC bits

+7	W	Write 8 higher DAC bits						
Bit #	7	6	5	4	3	2	1	0
Name	DAC15	DAC14	DAC13	DAC12	DAC11	DAC10	DAC9	DAC8

8 higher DAC bits.
 *Write leads to different results depending on the control bits status.
 If DASIM = 1, write occurs to memory cell with the DAC channel number, data output to DAC is not done.
 If DASIM = 0, current written value is additionally sent to DAC.
 If bit DAGEN = 1, the data are written to FIFO. This write to FIFO operation has priority over DASIM bit.

+8	R	Current page and power control						
Bit #	7	6	5	4	3	2	1	0
Name	0	PWREN	0	0	0	P2	P1	P0

Bits P2-0 set page for the mode of extended access to the ports of the module. The page consists of 4 registers and is mapped to 12-15 registers of the main IO area.
Bit PWREN = 1 – Power is supplied to analog part of the module (default value).

+8	W	Setting current page, power and module reset control						
Bit #	7	6	5	4	3	2	1	0
Name	0	PWREN	INTRST	RESETD	RESETA	P2	P1	P0

Bits P2-0 set page for the mode of extended access to the ports of the module. The page consists of 4 registers and is mapped to 12-15 registers of the main IO area.
Bit RESETA – Reset of DAC, FIFO, DIO and all internal registers. 8254 timer(s) is not reset.
Bit RESETD – The same reset as RESETA, but DAC is not affected.
Bit INTRST – Interrupts reset.
Bit PWREN = 1 – Power is supplied to analog part of the module (default value).

+9	R	Read galvanically isolated discrete inputs						
Bit #	7	6	5	4	3	2	1	0
Name	0	0	Debounce	DINTE	DIN3	DIN2	DIN1	DIN0

Bits DIN3-0 – Read discrete inputs at analog connector.
Bit DINTE – Enable interrupt from discrete IO.
Bit Debounce – Enable software debounce at Din[3] input. In case of bad signal, leads to possibility of the interrupt setting jitter of 6.4 microseconds max.

+9	W	Isolated discrete outputs control						
Bit #	7	6	5	4	3	2	1	0
Name	x	x	Debounce	DINTE	LED	DOUT2	DOUT1	DOUT0

Bits DOUT2-0 – Control of discrete outputs at analog connector.
Bit LED = 1, – Switch on the VD1 onboard LED.
Bit DINTE – Enable interrupt from discrete IO.
Bit Debounce – Enable software debounce at Din[3] input. In case of bad signal, leads to possibility of the interrupt setting jitter of 6.4 microseconds max.

+10	R/W	Timer 8254: clock and signal source control						
Bit #	7	6	5	4	3	2	1	0
Name	TINTE	GT12EN	SRC0	GT0EN	OUT0EN	OUT2EN	FREQ0	FREQ12
<p>Bit FREQ12 = 1, – Counter 1 input is supplied with 200 kHz signal from the internal generator; if = 0 – 20 MHz is supplied from the same source.</p> <p>Bit FREQ0 = 1, – Counter 0 input is supplied with 200 kHz signal from the internal generator; if = 0 – 20 MHz is supplied from the same source.</p> <p>Bit OUT2EN = 1, – Counter 2 output is routed to OUT2\DOUT2 output, cont. 42 of XP9 conn.</p> <p>Bit OUT0EN = 1, – Counter 0 output is routed to OUT0\DOUT0 output, cont. 44 of XP9 conn.</p> <p>Bit GT0EN = 1, – Gate0\DIN1 (cont. 47 of XP9) connected to timer 0. Active level is high. Pull-up to power 10 kohm.</p> <p>Bit SRC0 = 1, – Timer 0 receives clock freq. from FREQ0. = 0 – Clock input of the timer is connected to pin CLK0\DIN0 (cont. 48 of XP9). Active edge is negative. Pull-up to power 10 kohm.</p> <p>Bit GT12EN = 1 and if ExtGate\DIN2 (cont. 46 of XP9) = 0, then ADC conversion is started. ADC conversion is not started, if this pin = 1. If it was 0 at start and then set to 1, conversion pause is set until it is 1. Pull-up to power 10 kohm.</p> <p>Bit TINTE – Enable interrupt from 8254 timer.</p>								

+11	R/W	Interrupt flags read and reset						
Bit #	7	6	5	4	3	2	1	0
Name	x	x	x	x	x	ADINT	TINT	DINT
<p>Bit DINT = 1, interrupt received from discrete IO.</p> <p>Bit TINT = 1, interrupt received from 8254 timer.</p> <p>Bit ADINT = 1, interrupt received from ADC.</p> <p>Writing 1 in the correspondent bit resets the flag. To reset all flags, write 0xFF.</p>								

3.4 Page 0 – 8254 Timer

+12	R/W	Read/write counter 0 data
+13	R/W	Read/write counter 1 data
+14	R/W	Read/write counter 2 data
+15	R/W	8254 counter control port

Operation modes and registers fully comply with 8254 timer counter. For details, see standard description, for example at: <http://www.digchip.com/datasheets/parts/datasheet/227/8254.php>

3.5 Page 1 – 8255 IO Port

+12	R\W	Port A read/write
+13	R\W	Port B read/write
+14	R\W	Port C read/write
+15	R\W	Control port read/write

Operation modes and registers fully comply with Intel 8255 chip. For details, see standard description, for example at: http://en.wikipedia.org/wiki/Intel_8255



Attention! All ports support mode 0. Mode 1 is supported only by Port A; in mode 1 external synchronization outputs are connected to separate discrete connector pins, but not to port C as it is described in 8255 configuration.



Attention! Additional discrete port D has data direction connected with port C of 8255. I.e. outputs D3-D0 have similar direction with lower part of port C (C3-C0), outputs D5 – D4 have similar direction with upper part of port C (C7 –C4).

3.6 Page 2 – ADC Control

+12	W	Low byte of the threshold value for the FIFO						
Bit #	7	6	5	4	3	2	1	0
Name	FT8	FT7	FT6	FT5	FT4	FT3	FT2	FT1
Bits FT8-1 – FIFO threshold, at which an interrupt is generated to sample ADC data from FIFO.								

+12	R	Low byte of the word indicating current data quantity in FIFO						
Bit #	7	6	5	4	3	2	1	0
Name	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
Bits FC7-0 – Low byte of the word indicating current data quantity in FIFO.								

+13	R\W	High address of the threshold value for the FIFO						
Bit #	7	6	5	4	3	2	1	0
Name	x	x	x	x	x	x	FT10	FT9
Bits FT10 – 9 – FIFO threshold, at which an interrupt is generated to sample ADC data from FIFO. FIFO size is 2048 words.								

+13	R	High byte of the word indicating current data quantity in FIFO						
Bit #	7	6	5	4	3	2	1	0
Name	0	0	0	0	FC11	FC10	FC9	FC8
Bits FC11 – 8 – High byte of the word indicating current data quantity in FIFO. FIFO size is 2048 words.								

+14	R/W	ADC clock control						
Bit #	7	6	5	4	3	2	1	0
Name	x	x	x	x	x	CLKSEL	CLKEN	DMAEN

Bit DMAEN – Enable DMA channel use when sampling ADC data using FIFO.
 Bit CLKEN – Enable ADC conversion start clocking. If = 0, ADC start is possible only by writing to appropriate bit of the register.
 Bit CLKSEL = 0, ADC start with the negative edge from DIN3\EXTCLK. If = 1, start with the negative edge from 8254 timer/counter 2 output. 8254 timer/counter 2 works together with counter 1 of 8254.

+15	R/W	ADC conversion parameters setup						
Bit #	7	6	5	4	3	2	1	0
Name	RANGE	ADBU	G1	G0	SCINT1	SCINT0	SD1	SD0

Bits SD1-0 – Set ADC input switches operation mode. 0 – Diff. inputs, 1 – General. Bit 0 sets parameters for channels 0-7 and 16-23, bit 1 – for 8-15 and 24-31. Bit 0 is controlled by jumper J21, bit 1 – by J22. Open jumper corresponds to log. 1.
 Bits SCINT1-0 – Set interval for switching channels in scan mode. 00 – 20 μs, 01 – 15 μs, 10 – 10 μs, 11 – 4 μs.
 Bits G1-G0 – Set the gain for ADC route from 1 to 8.
 Bits RANGE and ADBU set ADC operation mode.
 RANGE = 1 – ADC conversion range 10V, = 0 – ADC conversion range 5V.
 ADBU = 1 – bipolar conversion mode, = 0 – unipolar.

3.7 Page 4 – Additional Discrete Port

+12	R	Read FPGA outputs from additional port D						
Bit #	7	6	5	4	3	2	1	0
Name	0	0	D5	D4	D3	D2	D1	D0

Bits D5-0 – Read FPGA outputs of add. port D. Port D input/output direction is defined by output direction of high and low port C registers (8255). Direction of low part of port C defines direction for registers D3..0. Direction of high part of port C defines direction for registers D5..4.

+12	W	Write data to additional port D						
Bit #	7	6	5	4	3	2	1	0
Name	x	x	D5	D4	D3	D2	D1	D0

Bits D5-0 – Write to additional port D. Port D input/output direction is defined by output direction of high and low port C registers (8255). Direction of low part of port C defines direction for registers D3..0. Direction of high part of port C defines direction for registers D5..4.

3.8 Page 5 – DAC Control

+12	R/W	Lower DAC buffer address						
Bit #	7	6	5	4	3	2	1	0
Name	DACA7	DACA6	DACA5	DACA4	DACA3	DACA2	DACA1	DACA0
Bits DACA7-0 – Address for writing DAC data into the signal generator circle buffer using DAC. Buffer length is 1024 DAC counts. Code and DAC channel number are written.								

+13	R/W	Higher DAC buffer address						
Bit #	7	6	5	4	3	2	1	0
Name	x	x	x	x	x	x	DACA9	DACA8
Bits DACA9-8 – Address for writing DAC data into the signal generator circle buffer using DAC. Buffer length is 1024 DAC counts. Code and DAC channel number are written.								

+14	R/W	Set the signal generator (DAG) operation mode						
Bit #	7	6	5	4	3	2	1	0
Name	WGSR1	WGSR0	WGCH1	WGCH0	DEPTH3	DEPTH2	DEPTH1	DEPTH0
<p>Bits DEPTH 3-0 – Set buffer size in use. Depth = [DEPTH(3-0)+1]*64.</p> <p>Bits WGCH1-0 – Set the number of words transmitted to DAC at a time. 00 – 1 word, 01 – 2 words, 1x – 4 words.</p> <p>Bits WGSR1-0 – Set DAC clock source. 00 – manual, WGINC register is used; 01 – 8254 counter 0 output, 10 – 8254 counter 12 output, 11 – external, pin 45.</p>								

+15	R/W	Set DAC configuration						
Bit #	7	6	5	4	3	2	1	0
Name		DAC_off	DAG1_1	DAG1_0	DAG0_1	DAG0_0	DAPOL1	DAPOL0
<p>Bit DAPOL1-0 = 1, bipolar DAC outputs 2-3 and 0-1 respectively.</p> <p>Bit DAG1_1-0 (DAG0_1-0) – Selection of DAC conversion range 2-3 (0-1). 00 – 5V, 01 – 10V, 10 – 20V, 11 – DAC disabled. *See also ranges switching rules.</p> <p>Bit DAC_OFF – Setting to 1 leads to disconnection of DAC outputs and grounding them via 10 kohm resistors.</p>								

3.9 Registers Summary

Base +	Read	Write
+0	Reading ADC data, lower byte	ADC conversion software start.
+1	Reading ADC data, higher byte	
+2	Low ADC channel number in scan mode	Low ADC channel number in scan mode
+3	High ADC channel number in scan mode	High ADC channel number in scan mode
+4	FIFO flags + ADC status	ADC control
+5	DAC status	DAC control
+6	Update of data in all 4 DAC channels	DAC low byte
+7		DAC high byte
+8	Current page	System module control
+9	Read discrete port	Interrupts and discrete port control
+10	8254 timer status	8254 timer inputs/outputs control
+11	Interrupts flags	Reset interrupts flags
	Page 0 – 8254 timer	
+12	Counter 0 data read	Counter 0 data write
+13	Counter 1 data read	Counter 1 data write
+14	Counter 2 data read	Counter 2 data write
+15	Control port read	Control port write
	Page 1 – 8255 IO port	
+12	Port A read	Port A write
+13	Port B read	Port B write
+14	Port C read	Port C write
+15	Control port read	Control port write
	Page 2 – ADC control	
+12	Low FIFO address	Low FIFO address
+13	High FIFO address	High FIFO address
+14	ADC clock control	ADC clock control
+15	Set ADC parameters	Set ADC parameters
	Page 3 – Access to calibration parameters	
	Page 4 – Additional discrete port	
+12	Additional discrete port read	Additional discrete port write
	Page 5 – DAC control	
+12	Low DAC buffer address	Low DAC buffer address
+13	High DAC buffer address	High DAC buffer address
+14	DAC operation modes	DAC operation modes
+15	DAC outputs setup	DAC outputs setup
	Page 6 – FPGA loader programming	

Appendix

Jumpers Functions

Jumper	Function
J1	DACK3
J2	DRQ3
J3	DACK1
J4	DRQ1
J5	IRQ7
J6	IRQ6
J7	IRQ5
J8	IRQ4
J9	Interrupt setting. It is set, if this module is sole at this interrupt.
J10	IRQ3
J11	IRQ14
J12	IRQ15
J13	IRQ12
J14	IRQ11
J15	IRQ10
J16	A0, setting the base address of the module
J17	A1, setting the base address of the module
J18	A2, setting the base address of the module
XP15	Connection of digital I/O: position 1-2 – pull up to power, 2-3 – pull down to ground.
J21	SD0 bit of ADC configuration, register 15 of page 2, logical “1” if the jumper is not closed.
J22	SD1 bit of ADC configuration, register 15 of page 2, logical “1” if the jumper is not closed.

Selection of the base address of the module:

J16	J17	J18	Base address (hex)
-	+	-	0x100
-	-	-	0x140
+	+	-	0x180
-	-	+	0x200
+	-	+	0x280
-	+	+	0x300
+	-	-	0x340
+	+	+	0x380

«+» – jumper closed, «-» – jumper open.